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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
TABONE JR, JOHN J	

ART UNIT	PAPER NUMBER
2117	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/714,026	VOGT, PETE D.	
	Examiner	Art Unit	
	John J. Tabone, Jr.	2117	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 May 2007 and 08 November 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9 and 11-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *19-27* is/are allowed.

6)☒ Claim(s) *1-9,11-18 and 28-34* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 August 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *11082007*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-9 and 11-34 are pending in the current application and has been examined.

Response to Arguments

2. Appellant's arguments filed in the Appeal Brief of 05/14/2007 with respect to claims 2-5, 7, 12 and 17 have been considered but are moot in view of the new ground(s) of rejection.

Further, Appellant did not argue nor appeal independent claims 1 and 28 and, as such, has conceded to the validity of the rejection. Therefore, the rejections of claims 1 and 28-34 are maintained without further response from the Examiner.

Information Disclosure Statement

3. The information disclosure statement filed 11/08/2007 fails to comply with the provisions of 37 CFR 1.97, 1.98 and MPEP § 609 because the Foreign Patent and Non-Patent Literature documents were already considered in the IDS filed 02/09/2006. It has been placed in the application file, but the information referred to therein has not been considered as to the merits. Applicant is advised that the date of any re-submission of any item of information contained in this information disclosure statement or the submission of any missing element(s) will be the date of submission for purposes of determining compliance with the requirements based on the time of filing the

statement, including all certification requirements for statements under 37 CFR 1.97(e). See MPEP § 609.05(a).

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 3-7, 12-18 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 3-7, 12, 15-17:

These claims recite the phrases “may operate”, "may selectively map", "may retransmit", "may transmit, receive, analyze", etc.. The use of the word "may" renders these claims indefinite because the claim language does not definitively claim whether the memory agent does or does not perform a particular operation. Clarification and correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States

only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 12-18 are rejected under 35 U.S.C. 102(e) as being anticipated by Bunton et al. (US006961347), hereinafter Bunton.

Claim 12:

Bunton teaches a first link interface having a plurality of first lanes; and a second link interface having a plurality of second lanes. (two lane links 140, Fig. 2, col. 6, ll. 59-65, col. 10, ll. 24-26). Bunton also teaches the memory agent (computer 100/server 300, network switch 130, Fig. 2, 3) may transmit training sequences having different mapping indicators on one or more of the plurality of first lanes, receive return sequences on one or more of the plurality of second lanes responsive to the training sequences and analyzing the return sequences to identify failed lanes in the plurality of first lanes and plurality of second lanes. Bunton does teach a memory agent in that Bunton's invention is for the solution of I/O problems between processors, memory controllers and memory in a memory-processor architecture. Also, in reference to Fig. 3 Bunton teaches [a]lternatively, the HCA 220 may be connected directly to a memory controller 204 (memory agent). (Abstract, Col. 4, ll. 18-54, col. 7, l. 18 to col. 9, l. 8, Fig. 4-6, col. 10, l. 29 to col. 12, l. 8, Fig. 9-12).

Claim 13:

Bunton teaches the first link interface comprises a receive link interface and the second link interface comprises a transmit link interface. (two lane links 140, Fig. 2, col. 6, ll. 59-65, col. 10, ll. 24-26).

Claim 14:

Bunton teaches the first lanes comprise receive bit lanes and the second lanes comprise transmit bit lanes. (two lane links 140, Fig. 2, col. 6, ll. 59-65, col. 10, ll. 24-26).

Claim 15:

Bunton teaches the memory agent may receive the training sequences as the return sequences. (Abstract, Col. 4, ll. 18-54, col. 7, l. 18 to col. 9, l. 8, Fig. 4-6, col. 10, l. 29 to col. 12, l. 8, Fig. 9-12).

Claim 16:

Bunton teaches the memory agent may transmit test parameters in the training sequences. (Abstract, Col. 4, ll. 18-54, col. 7, l. 18 to col. 9, l. 8, Fig. 4-6, col. 10, l. 29 to col. 12, l. 8, Fig. 9-12).

Claim 17:

Bunton teaches the memory agent may transmit electrical stress patterns in the training sequences. (Abstract, Col. 4, ll. 18-54, col. 7, l. 18 to col. 9, l. 8, Fig. 4-6, col. 10, l. 29 to col. 12, l. 8, Fig. 9-12).

Claim 18:

Bunton teaches the memory agent comprises a memory controller. (NORTH BRIDGE 206, alternately a memory controller, col. 7, ll. 9-10).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-9, 11, 28-34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bunton et al. (US006961347), hereinafter Bunton, in view of Li et al. (US-5515361), hereinafter Li.

Claim 1:

Bunton teaches a receive link interface having a plurality of receive lanes to receive training sequences and a transmit link interface having a plurality of transmit lanes to transmit training sequences. (two lane links 140, Fig. 2, col. 6, ll. 59-65; col. 10, ll. 24-26). (Abstract, Col. 4, ll. 18-54, Col. 10, l. 29 to col. 12, l. 8, Fig. 9-12). Bunton also teaches a memory agent in that Bunton's invention is for the solution of I/O problems between processors, memory controllers and memory in a memory-processor architecture. Also, in reference to Fig. 3 Bunton teaches [a]lternatively, the HCA 220 may be connected directly to a memory controller (memory agent). (Col. 2, ll. 17-35, col. 6, l. 66 to col. 7, l. 10).

Bunton does not explicitly teach "a loopback unit coupled to the receive and transmit link interfaces to selectively redirect one or more of the receive lanes to one or more of the transmit lanes to retransmit the received training sequences as the return sequences during a lane testing operation". Li teaches in an analogous art "a loopback

unit (**loopback switch 301**) coupled to the receive (**receiver 202**) and transmit (**transmitter 201**) link interfaces to selectively redirect (**loop 306**) one or more of the receive lanes (**up link 206**) to one or more of the transmit lanes (**down link 207**) to retransmit the received training sequences as the return sequences during a lane testing operation". (Fig. 2, 3A, 3B, col. 3, ll. 11-60). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Bunton's multi-lane link system to incorporate Li's loopback switch 301. The artisan would be motivated to do so because it would enable Bunton to loopback the transmit links to the receive links upon detecting a training sequence failure and further enable Bunton to facilitate failure isolation in a bus architecture (see Bunton, col. 8, ll. 4-12 for problem to be solved and Li, col. 3, ll. 41-60 for solution to Bunton's problem).

Claim 2:

Bunton teaches the receive link interface is a first receive link interface and the transmit link interface is a first transmit link interface. (multi-lane links 140, Fig. 2, col. 6, ll. 59-65, col. 10, ll. 24-26, Fig. 9).

Bunton does not explicitly disclose a second transmit link interface having a plurality of second transmit lanes and a second receive link interface having a plurality of second receive lanes. However, Bunton does teach a multi-lane links 140 in Fig. 2 an d Fig. 9. It would have been obvious to one of ordinary skill in the art at the time the invention was made to duplicate two lane links 140. The artisan would be motivated to do so because since it has been held that mere duplication of the essential working

parts of a device involves only routine skill in the art. *St. Regis Paper Co. v. Bemis Co.*, 193 USPQ 8 (7th Cir. 1977).

Claim 3:

Bunton in view of Li teaches a passthrough mode during a lane testing operation by retransmitting training sequences received on the first receive link interface to the second transmit link interface, and retransmitting retum sequences received on the second receive link interface to the first transmit link interface. (Fig. 2, 3A, col. 3, ll. 35-40, in the normal mode of operation of the loopback switch 301, optical switch 208 is set in the `bar` position 302).

Claim 4:

Bunton teaches the memory agent may selectively map one of the receive lanes to one or more of the transmit lanes during a lane testing operation. (Abstract, Col. 4, ll. 18-54, col. 7, l. 18 to col. 9, l. 8, Fig. 4-6, col. 10, l. 29 to col. 12, l. 8, Fig. 9-12).

Claim 5:

Bunton teaches the memory agent may selectively map one or more of the receive lanes to one or more of the transmit lanes according to a plurality of mappings. (Abstract, Col. 4, ll. 18-54, col. 7, l. 18 to col. 9, l. 8, Fig. 4-6, col. 10, l. 29 to col. 12, l. 8, Fig. **9**-12).

Claim 6:

Bunton teaches memory agent may select one of the mappings responsive to a mapping indicator in a training sequence received on the receive link interface.

(Abstract, Col. 4, ll. 18-54, col. 7, l. 18 to col. 9, l. 8, Fig. 4-6, col. 10, l. 29 to col. 12, l. 8, Fig. 9-12).

Claim 7:

Bunton teaches the memory agent may retransmit the received training sequence with modification as the return sequence. (Abstract, Col. 4, ll. 18-54, col. 7, l. 18 to col. 9, l. 8, Fig. 4-6, col. 10, l. 29 to col. 12, l. 8, Fig. 9-12).

Claim 8:

Bunton teaches the memory agent comprises a memory buffer (FIFO buffers, Fig. 8).

Claim 9:

Bunton teaches the memory agent comprises a memory module (memory 204, Fig. 3).

Claim 11:

Bunton in view of Li teaches the loopback unit (**loopback switch 301**), which comprises a multiplexer (**switch 208**).

Claim 32:

Bunton in view of Li teaches the modification includes identifying or status information. (two lane links 140, Fig. 2, col. 6, ll. 59-65, col. 10, ll. 24-26).

Claim 33:

Bunton in view of Li teaches one of the return sequences comprises one of the received training sequences. (two lane links 140, Fig. 2, col. 6, ll. 59-65, col. 10, ll. 24-26).

Claim 34:

Bunton in view of Li teaches one of the return sequences consists essentially of one of the received training sequences. (two lane links 140, Fig. 2, col. 6, ll. 59-65, col. 10, ll. 24-26).

Claim 28:

Bunton teaches a receice link interface having a plurality of receive lanes to receive training sequences and a transmit link interface having a plurality of transmit lanes to transmit training sequences. (two lane links 140, Fig. 2, col. 6, ll. 59-65, col. 10, ll. 24-26). Bunton also teaches a memory agent in that Bunton's invention is for the solution of I/O problems between processors, memory controllers and memory in a memory-processor architecture. Also, in reference to Fig. 3 Bunton teaches [a]lternatively, the HCA 220 may be connected directly to a memory controller (memory agent). (Col. 2, ll. 17-35, col. 6, l. 66 to col. 7, l. 10). Bunton further teaches a memory controller (NORTH BRIDGE 206, alternately a memory controller, col. 7, ll. 9-10) coupled to the memory agent. (Abstract, Col. 4, ll. 18-54, Col. 10, l. 29 to col. 12, l. 8, Fig. 9-12).

Bunton does not explicitly teach "a loopback unit coupled to the receive and transmit link interfaces to selectively redirect one or more of the receive lanes to one or more of the transmit lanes to retransmit the received training sequences as the return sequences during a lane testing operation". Li teaches in an analogous art "a loopback unit (**loopback switch 301**) coupled to the receive (**receiver 202**) and transmit (**transmitter 201**) link interfaces to selectively redirect (**loop 306**) one or more of the

receive lanes (**up link 206**) to one or more of the transmit lanes (**down link 207**) to retransmit the received training sequences as the return sequences during a lane testing operation". (Fig. 2, 3A, 3B, col. 3, ll. 11-60). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Bunton's multi-lane link system to incorporate Li's loopback switch 301. The artisan would be motivated to do so because it would enable Bunton to loopback the transmit links to the receive links upon detecting a training sequence failure and further enable Bunton to facilitate failure isolation in a bus architecture (see Bunton, col. 8, ll. 4-12 for problem to be solved and Li, col. 3, ll. 41-60 for solution to Bunton's problem).

Claim 29:

Bunton teaches the first link interface comprises a receive link interface and the second link interface comprises a transmit link interface. (two lane links 140, Fig. 2, col. 6, ll. 59-65, col. 10, ll. 24-26).

Claim 30:

Bunton teaches the first lanes comprise receive bit lanes and the second lanes comprise transmit bit lanes. (two lane links 140, Fig. 2, col. 6, ll. 59-65, col. 10, ll. 24-26).

Claim 31:

Bunton teaches a second memory agent coupled to the memory agent. (Fig. 7, col. 9, ll. 9-52).

Allowable Subject Matter

7. Claims 19-27 are allowed.

The Examiner agrees with the Applicant's arguments file 08/30/2006 with regard to the feature recited in independent claim 19 in view of the arts of record; therefore, the Examiner favors the allowance of claims 19-27. Any comments considered necessary by applicant must be submitted no later than the payment of the Issue Fee and, to avoid processing delays, should preferably accompany the Issue Fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John J. Tabone, Jr. whose telephone number is (571) 272-3827. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, JACQUES H. LOUIS JACQUES can be reached on (571) 272-6962. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

John J. Tabone, Jr.
Examiner
Art Unit 2117

1/31/08

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